WHAT IS CLAIMED IS:

1. A circuit for communicating signals, comprising:

a transmit amplification device for transmitting signals, the transmit amplification device including more than one amplification stage;

a receive amplification device for receiving signals, the receive amplification device including more than one amplification stage; and

an antenna connected to the amplification devices;

wherein the amplification devices both include in common one of the amplification stages as a joint amplification stage.

2. The circuit of Claim 1, wherein the joint amplification stage includes a symmetrical MOS transistor.

3. The circuit of Claim 2, wherein each of the amplification devices includes first and second said amplification stages, the first and second amplification stages of the transmit device operationally corresponding to the first and second amplification stages of the receive device, respectively, and wherein the joint amplification stage is the first amplification stage of the receive amplification device and is also the second amplification stage of the transmit amplification device.

4. The circuit of Claim 3, including a first switching device connected to one of the amplification stages of the transmit amplification device other than the

joint amplification stage for switching off the transmit amplification device while the receive amplification device is receiving signals, and a second switching device connected to one of the amplification stages of the receive amplification device other than the joint amplification stage for switching off the receive amplification device while the transmit amplification device is transmitting signals.

5. The circuit of Claim 4, wherein the receive amplification device has an input impedance that is matched to a load impedance of the transmit amplification device.

6. The circuit of Claim 3, wherein the receive amplification device has an input impedance that is matched to a load impedance of the transmit amplification device.

7. The circuit of Claim 2, including a first switching device connected to one of the amplification stages of the transmit amplification device other than the joint amplification stage for switching off the transmit amplification device while the receive amplification device is receiving signals, and a second switching device connected to one of the amplification stages of the receive amplification device other than the joint amplification stage for switching off the receive amplification device while the transmit amplification device is transmitting signals.

8. The circuit of Claim 7, wherein the receive amplification device has an input impedance that is matched to a load impedance of the transmit amplification device.

9. The circuit of Claim 2, wherein the receive amplification device has an input impedance that is matched to a load impedance of the transmit amplification device.

10. The circuit of Claim 1, wherein each of the amplification devices includes first and second said amplification stages, the first and second amplification stages of the transmit device operationally corresponding to the first and second amplification stages of the receive device, respectively, and wherein the joint amplification stage is the first amplification stage of the receive amplification device and is also the second amplification stage of the transmit amplification device.

11. The circuit of Claim 10, including a first switching device connected to one of the amplification stages of the transmit amplification device other than the joint amplification stage for switching off the transmit amplification device while the receive amplification device is receiving signals, and a second switching device connected to one of the amplification stages of the receive amplification device other than the joint amplification stage for switching off the receive amplification device while the transmit amplification device is transmitting signals.

12. The circuit of Claim 11, wherein the receive amplification device has an input impedance that is matched to a load impedance of the transmit amplification device.

13. The circuit of Claim 10, wherein the receive amplification device has an input impedance that is matched to a load impedance of the transmit amplification device.

14. The circuit of Claim 1, including a first switching device connected to one of the amplification stages of the transmit amplification device other than the joint amplification stage for switching off the transmit amplification device while the receive amplification device is receiving signals, and a second switching device connected to one of the amplification stages of the receive amplification device other than the joint amplification stage for switching off the receive amplification device while the transmit amplification device is transmitting signals.

15. The circuit of Claim 14, wherein the receive amplification device has an input impedance that is matched to a load impedance of the transmit amplification device.

16. The circuit of Claim 1, wherein the receive amplification device has an input impedance that is matched to a load impedance of the transmit amplification device.